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Development of Fault Diagnosis Equipment for High Speed Maglev Traction Converter System

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Abstract

This paper investigates the fault diagnosis technology of the high-speed maglev traction inverter system using IGCT three-level inverters. Due to the increase in output levels, the number of power devices increases. The circuit structure and control structure become more complex. Secondly, power devices withstand high voltage and current during operation, generate a large amount of heat, and accelerate the aging rate. This leads to degradation in component performance and reduced reliability, increasing the probability of failures. Therefore, improving the online monitoring and fault diagnosis technology of traction inverter systems is crucial for the safe, efficient, and reliable operation of high-speed maglev traction. This paper first establishes an accurate mathematical model and conducts simulation analysis of system operation characteristics under different fault conditions. It then proposes and designs power device fault feature extraction and localization methods suitable for different operating conditions. Finally, the design, development, and evaluation of fault diagnosis equipment for high-speed maglev train high-voltage, high-capacity threelevel traction inverter systems are completed, including analysis processing software, fault recognition software, and human-machine interface design.

Keywords: traction inverter system, fault diagnosis technology, IGCT three-level inverter, structural failure, parametric failure, experiment.

1 Introduction

The high-voltage high-capacity traction inverter system serves as the core critical system for high-speed maglev trains, providing the necessary power for their operation. The performance of this system plays a decisive role in ensuring the overall safety and reliability of the train's journey. Additionally, the system faces elevated demands due to harsh operating conditions such as long distances, high temperatures, and extreme cold. Comprising components like the input transformer, three-level traction inverter, output transformer, output switch cabinet, stator switch cabinet, and traction control unit. The high-speed maglev traction inverter system employs IGCT three-level inverters compared to traditional two-level inverters. The increase in voltage levels results in a sharp rise in the number of power devices, making the circuit and control structures more complex. Furthermore, these power devices operate under high voltage and large current, leading to increased heat generation and accelerated aging. Continuous operation further contributes to the degradation of component performance and reduced reliability, significantly raising the probability of failures. Consequently, the development of online monitoring and fault diagnosis technology for high-speed maglev traction inverter systems becomes crucial. This includes achieving system health diagnosis, fault prediction, fault recognition, fault cause analysis, and localization, all of which are essential for enhancing the safety, efficiency, and reliability of high-speed maglev traction operations.

Currently, the theoretical research on fault diagnosis technology for maglev traction inverter systems is still immature, with relatively few reports in domestic and international literature. The reasons for this are as follows. The fault information of the inverter generally only remains within the first few milliseconds of the fault occurrence, which requires high demands for real-time detection and online diagnosis of information. Ordinary digital circuits change the input to reflect changes in the output, but for high-voltage high-capacity traction inverter systems, with large working currents and high voltages, fault diagnosis can only be achieved through output waveforms. In complex inverter circuits with numerous power switch devices, diagnosing each device individually is time-consuming and laborious, with poor practicality^[1-3].

With the deepening development of intelligent algorithms, various combined fault diagnosis methods have emerged. Commonly used methods include wavelet fuzzy algorithms, wavelet fuzzy neural network algorithms, wavelet adaptive fuzzy neural inference, clustering adaptive fuzzy neural inference algorithms, and so on. The wavelet fuzzy algorithm diagnoses inverter faults by real-time monitoring of three-phase currents. Specifically, wavelet analysis detects changes in the current and calculates the direct current offset component^[4]. The fuzzy algorithm uses the polarity and amplitude of the direct current offset component as inputs and diagnoses whether an inverter open circuit fault has occurred based on preset rules. Both the wavelet neural network algorithm and the wavelet fuzzy expert system algorithm obtain three-phase current fault characteristic quantities through wavelet transformation^[5]. They use artificial intelligence neural network algorithms or fuzzy expert system methods to classify fault patterns and diagnose inverter faults. The wavelet adaptive fuzzy

neural inference algorithm detects inverter faults by monitoring direct current busbar currents and uses wavelet transformation to obtain fault characteristics. The adaptive fuzzy neural inference algorithm is responsible for training the diagnostic mechanism. The fuzzy logic algorithm enables the fault algorithm to adapt to the nonlinear behavior of control system parameters. The clustering adaptive fuzzy neural inference algorithm first transforms the three-phase current coordinates into dq-axis coordinates and uses clustering adaptive fuzzy neural inference algorithms for fault recognition. This method reduces the dimensionality of the fuzzy model, decreases training time, and lowers misdiagnosis rates^[6-7].

This study aims to address the contradiction between the lagging development of fault diagnosis technology for traction inverter systems and the high safety and reliability requirements of China's rail transit industry. Firstly, an accurate mathematical model of the high-speed maglev traction inverter system is established. The study analyzes the current flow paths and output voltage characteristics of the traction inverter system under different types of open circuit and short circuit faults, followed by simulation analysis of the system's operation characteristics under fault conditions. Next, a method for extracting and locating power device faults suitable for various operating conditions of high-speed maglev traction inverter systems is proposed. Diagnostic algorithms for grid-side power supply faults, transformer faults, sensor faults, and midpoint voltage imbalance faults are designed. Finally, by constructing a high-precision, high-sampling-rate, and high-reliability signal conditioning circuit and data acquisition system, the study completes the design, development, and evaluation of fault diagnosis equipment for high-speed maglev train high-voltage, high-capacity three-level traction inverter systems, including analysis processing software, fault recognition software, and human-machine interface design.

2 Fault Mechanism Modeling Research

The high-speed maglev traction inverter system adopts a three-level NPC (Neutral Point Clamped) topology, as shown in Figure 1, where only one-phase DC di/dt limiting circuit is depicted for illustration. The three-level inverter can be represented by three-state switch variables S_A , S_B , S_C , corresponding to the three switch states of each bridge arm. The variable S_A represents the switch state of bridge arm A. If switches S_{A3} and S_{A4} in bridge arm A are conducting while S_{A1} and S_{A2} are turned off, the equivalent circuit is shown in Figure 2 (a), defining this state as -1 state, i.e., $S_A = -1$, and $v_{AO} = -V_{dc}/2$. If switches S_{A2} and S_{A3} in bridge arm A are conducting while S_{A1} and S_{A2} in bridge arm A are conducting while S_{A1} and S_{A2} in bridge arm A are conducting while S_{A1} and S_{A4} are turned off, the equivalent circuit is shown in Figure 2 (b), defining this state as 0 state, i.e., $S_A = 0$, and $v_{AO} = 0$. If switches S_{A1} and S_{A2} in bridge arm A are conducting while S_{A3} and S_{A4} are turned off, the equivalent circuit is shown in Figure 2 (b), defining this state as 0 state, i.e., $S_A = 0$, and $v_{AO} = 0$. If switches S_{A1} and S_{A2} in bridge arm A are conducting while S_{A3} and S_{A4} are turned off, the equivalent circuit is shown in Figure 2 (b), defining this state as 0 state, i.e., $S_A = 0$, and $v_{AO} = 0$. If switches S_{A1} and S_{A2} in bridge arm A are conducting while S_{A3} and S_{A4} are turned off, the equivalent circuit is shown in Figure 2 (c), defining this state as 1 state, i.e., $S_A = 1$, and $v_{AO} = V_{dc}/2$.

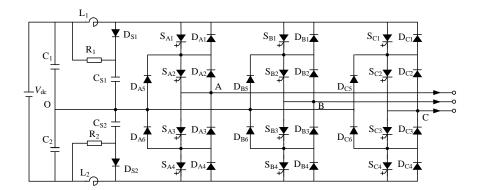


Figure 1: The three-phase three-level inverter topology

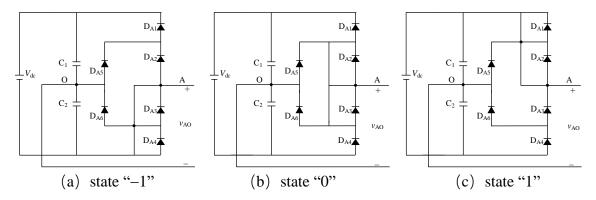


Figure 2: The equivalent circuit of phase A in a three-level inverter.

The three-phase three-level inverter consists of twelve IGCTs, six clamping diodes, and two DC-side capacitors, with each IGCT requiring additional anti-parallel diodes at its ends. In extreme cases, each IGCT could potentially fail, resulting in a total of $(2^{12} - 1)$ possible fault scenarios. However, it is evident that in practical situations, the probability of two or more power devices simultaneously experiencing open circuit faults in the inverter is relatively low. Therefore, this report focuses on single-switch open circuit faults for investigation.

(a)Single-switch open circuit fault

In the case of single-switch open circuit fault, any one of the power devices S_{k1} , S_{k2} , S_{k3} , S_{k4} (k=A, B, C) in the A, B, C phase bridge arms may experience an open circuit fault, resulting in a total of 12 fault modes. Taking the S_{A1} open circuit fault as an example, under the single-switch S_{A1} open circuit fault, the B and C phase circuits in the three-phase inverter remain unaffected and operate normally, while only the topology of the A phase circuit may change under certain conditions. When $S_A=0$ (0 state) or $S_A=-1$ (-1 state), the S_{A1} open circuit fault does not affect the output of phase A. However, when $S_A=1$ and $i_A \ge 0$, the SA1 open circuit fault leads to a change in the current flow path, affecting the output of phase A (refer to Figure 1. On the other hand, when $S_A=1$ and $i_A<0$, the S_{A1} open circuit fault does not impact the output of phase A. Under the single-switch S_{A1} open circuit fault, v_{AO} is

$$v_{AO} = \begin{cases} 0 , S_{A} = 1, i_{A} \ge 0 \\ \frac{S_{A}V_{dc}}{2} , S_{A} = 1, i_{A} < 0 \\ \frac{S_{A}V_{dc}}{2} , S_{A} = 0 \\ \frac{S_{A}V_{dc}}{2} , S_{A} = -1 \end{cases}$$
(1)

(b) Single-switch short circuit fault

The impact of single-switch short circuit faults on the v_{kO} voltage is summarized in Table 1. Taking S_{k1} short circuit as an example, the content in the table is explained as follows: When $S_A=0$ and S_{k1} is healthy, $v_{kO}=0$; however, when S_{k1} experiences a short circuit fault, it causes a short circuit in capacitor C_1 , i.e., the upper half-bridge on the DC side is short-circuited. When $S_A=-1$ and S_{k1} is healthy, $v_{kO}=-V_{dc}/2$; but when Sk1 experiences a short circuit fault, it causes a short circuit fault, it causes a short circuit and C_2 , i.e., the entire bridge on the DC side is short-circuited. Additionally, the symbol "--" in the table indicates that whether the device is short-circuit or not under the corresponding condition does not cause a change in v_{kO} or a short circuit in the DC capacitor.

Variation of v_{ko}		$S_k=1$	$S_k=0$	S _k =-1	
	\mathbf{S}_{k1}		Upper bridge short circuit	Full-bridge short circuit	
Short- circuit device	\mathbf{S}_{k2}			Lower bridge short circuit	
	\mathbf{S}_{k3}	Upper bridge short circuit			
	\mathbf{S}_{k4}	Full-bridge short circuit	Lower bridge short circuit		

Table 1: Voltage Variation of v_{kO} (k=A, B, C) Before and After Single-Switch Short Circuit Fault

3 Extraction and Localization of Fault Features

3.1 Structural failure

(a) Open circuit fault of power devices

Assuming the power device is an ideal switch. According to the working principle of the inverter, the line voltage is estimated using the DC bus voltage and power transistor switch signal. The calculation method is shown in formula 2.

$$\begin{cases} v_{AB_{e}e} = \frac{1}{2} V_{dc} (S_{A} - S_{B}) \\ v_{BC_{e}e} = \frac{1}{2} V_{dc} (S_{B} - S_{C}) \\ v_{CA_{e}e} = \frac{1}{2} V_{dc} (S_{C} - S_{A}) \end{cases}$$
(2)

where the DC bus voltage is represented by V_{dc} . S_A , S_B and S_C represent the switching status of each phase of the inverter. When $S_i=1$, it indicates that S_{x1} and S_{x2} are activated, while S_{x3} and S_{x4} are deactivated. When $S_i=0$, it indicates that S_{x2} and S_{x3} are activated, while S_{x1} and S_{x4} are deactivated. When $S_i=-1$, it indicates that S_{x3} and S_{x4} are activated, while S_{x1} and S_{x2} are deactivated. When $S_i=-1$, it indicates that S_{x3} and S_{x4} are activated, while S_{x1} and S_{x2} are deactivated. I is either A or B or C.

The measured output phase voltage of the inverter is defined as v_{AO-act} , v_{BO-act} and v_{CO-act} . The calculation of error line voltage is shown in formula 3.

$$\begin{bmatrix} \Delta \mathbf{v}_{AB} \\ \Delta \mathbf{v}_{BC} \\ \Delta \mathbf{v}_{CA} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} \mathbf{v}_{AO_act} \\ \mathbf{v}_{BO_act} \\ \mathbf{v}_{CO_act} \end{bmatrix} - \begin{bmatrix} \mathbf{v}_{AB_e} \\ \mathbf{v}_{BC_e} \\ \mathbf{v}_{CA_e} \end{bmatrix}$$
(3)

According to formulas (2) and (3), the amplitude of the error line voltage under the opencircuit fault type can be calculated. The results are shown in Table 2.

Power	Normal	Open circuit fault				
devices	$\Delta v_{ m AB,BC,CA}$	$\Delta v_{ m AB}$	$\Delta v_{ m BC}$	$\Delta v_{ m CA}$		
S_{A1}		$-V_{\rm dc}/2$	0	$V_{\rm dc}/2$		
S_{A2}		$-V_{ m dc}$	0	$V_{ m dc}$		
S _{A3}		$V_{ m dc}$	0	$-V_{ m dc}$		
$S_{\rm A4}$	0	$V_{\rm dc}/2$	0	$-V_{ m dc}/2$		
S_{B1}		$V_{\rm dc}/2$	$-V_{\rm dc}/2$	0		
$S_{\rm B2}$		$V_{ m dc}$	$-V_{ m dc}$	0		
$S_{\rm B3}$		$-V_{ m dc}$	$V_{ m dc}$	0		
$S_{\rm B4}$		$-V_{\rm dc}/2$	$V_{\rm dc}/2$	0		
S_{C1}		0	$V_{\rm dc}/2$	$-V_{ m dc}/2$		
S _{C2}		0	$V_{ m dc}$	$-V_{ m dc}$		
S _{C3}		0	$-V_{ m dc}$	$V_{ m dc}$		
S_{C4}		0	$-V_{\rm dc}/2$	$V_{\rm dc}/2$		

Table 2: Error line voltage amplitude under open circuit fault ($\cos \varphi = 1$).

As shown in the table above, using the amplitude and polarity of the error line voltage as the fault characteristic values can achieve open circuit fault localization. In addition, as the output voltage of the inverter depends on the DC bus voltage and the driving pulse signal of the power device, it is not affected by the power factor.

(b) Short circuit fault of power devices

Power	Normal	Short circuit fault				
devices	$\Delta v_{ m AB,BC,CA}$	$\Delta v_{ m AB}$	$\Delta v_{ m BC}$	$\Delta v_{ m CA}$		
$S_{ m A1}$		$V_{\rm dc}/4$	0	$-V_{\rm dc}/4$		
$S_{ m A2}$		$V_{\rm dc}//4$	0	$-V_{\rm dc}//4$		
$S_{\rm A3}$		$-V_{\rm dc}/4$	0	$V_{\rm dc}/4$		
$S_{ m A4}$	0	-V _{dc} //4	0	V _{dc} //4		
$S_{\rm B1}$		$-V_{\rm dc}/4$	$V_{\rm dc}/4$	0		
$S_{\rm B2}$		-V _{dc} //4	V _{dc} //4	0		
$S_{\rm B3}$		$V_{\rm dc}/4$	$-V_{\rm dc}/4$	0		
$S_{ m B4}$		V _{dc} //4	$-V_{\rm dc}//4$	0		
$S_{\rm C1}$		0	$-V_{\rm dc}/4$	$V_{\rm dc}/4$		
$S_{\rm C2}$		0	$-V_{\rm dc}//4$	V _{dc} //4		
S _{C3}		0	$V_{\rm dc}/4$	$-V_{\rm dc}/4$		
$S_{\rm C4}$		0	V _{dc} //4	$-V_{\rm dc}//4$		

According to formulas (2) and (3), the amplitude of the error line voltage under the short circuit fault type can be calculated. The results are shown in Table 3.

Table 3: Error line voltage amplitude under short circuit fault ($\cos\varphi=1$).

As shown in the table above, using the amplitude and polarity of the error line voltage as the fault characteristic values can achieve short circuit fault localization. But it can only locate which bridge arm fault, and cannot locate which component fault.Similarly, since the output voltage of the inverter depends on the DC bus voltage and the driving pulse signal of the power device, it is not affected by the power factor.

(c) Short circuit fault of transformer

For example, when a short circuit fault occurs in phase AB, when the input transformer currents i_A and i_B are both greater than 150% of the rated current and last for more than 5ms, a high level is output through a trigger to indicate that the transformer has a short circuit fault.

(d) Phase missing fault of the grid

Taking phase A as an example, when the grid side current i_A is less than 3% of the rated current and lasts for more than 5ms, and the difference between the absolute values of i_B and i_C is less than 3% of the rated current and lasts for more than 5ms, the trigger outputs a high level, indicating that phase A on the power grid side is missing.

3.2 Parametric failure

(a) Low voltage fault of the grid

When the grid voltage is less than 85% of the rated voltage and the duration is greater than 5ms, a high level is output through a trigger. If the duration of this high level is greater than 10ms, it is a power supply flicker (too low) fault. If the duration of this high level is greater than 20ms, it is a low voltage fault of the grid.

(b) High voltage fault of the grid

When the grid voltage is greater than 115% of the rated voltage and the duration is greater than 5ms, a high level is output through a trigger. If the duration of this high level is greater than 10ms, it is a power supply flicker (too high) fault. If the duration of this high level is greater than 20ms, it is a high voltage fault of the grid.

(c) Imbalance fault of midpoint voltage

When the deviation of the DC side midpoint voltage is greater than 10% of the DC side voltage and the duration exceeds 5ms, the fault diagnosis algorithm sends a high-level signal through a trigger to indicate the occurrence of a midpoint voltage imbalance fault.

4 Experiment

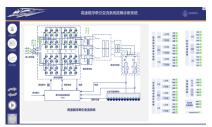
Based on the theoretical analysis results in the previous section, the NI cRIO platform is selected as the hardware data acquisition part. LabView software was used to develop fault diagnosis algorithms and upper computer interaction interfaces. A fault diagnosis equipment has been developed, as shown in the following figure.



(a)Hardware data acquisition equipment



(b)Fault diagnosis algorithms



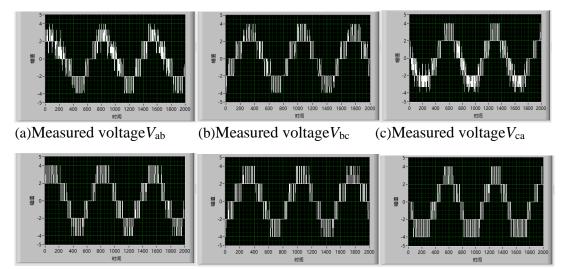
(b) Upper computer interaction interfaces

Figure 3: A fault diagnosis equipment.

To evaluate the performance of fault diagnosis equipment and verify the reliability of fault diagnosis algorithms, a testing environment was built based on RT Lab simulation machine and NI cRIO controller.

Taking inverter S_{A1} as an example, simulate an open circuit fault. Figure 4 shows the measured and reference values of the line voltage. From the figure, it can be seen

that after an open circuit fault occurred in S_{A1} , the line voltages V_{ab} and V_{ca} showed distortion, and the error line voltage Δv_{AB} and Δv_{CA} is no longer zero. Figure 5 shows the results of the fault flag bits. In the figure, the fault flag bit fa of phase A is 1, the fault flag bit fa1 of the upper bridge arm is 1, and the other fault flag bits are 0. The results are correct.



(e)Reference voltage V_{ab_ref} (f)Reference voltage V_{bc_ref} (g)Reference voltage V_{ca_ref}

Figure 4: A fault diagnosis equipment.

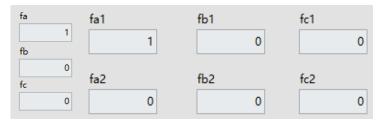
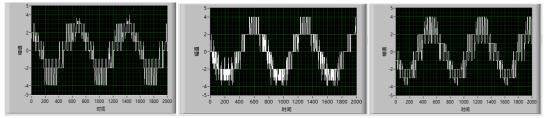


Figure 5: Inverter fault flag during S_{A1} open circuit fault.

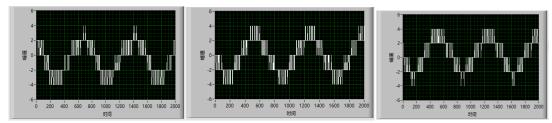
Taking inverter S_{A1} as an example, simulate an short circuit fault. Figure 6 shows the measured and reference values of the line voltage. From the figure, it can be seen that after an short circuit fault occurred in S_{A1} , the line voltages V_{ab} and V_{ca} showed distortion, and the error line voltage Δv_{AB} and Δv_{CA} is no longer zero. Figure 7 shows the results of the fault flag bits. In the figure, the fault flag bit fa of phase A is 1, the fault flag bit fa1 of the upper bridge arm is 1, and the other fault flag bits are 0. The results are correct.



(a)Measured voltage V_{ab}

(b)Measured voltage V_{bc} (c)Meas

(c)Measured voltage V_{ca}



(e)Reference voltage V_{ab_ref} (f)Reference voltage V_{bc_ref} (g)Reference voltage V_{ca_ref}

Figure 6: A fault diagnosis equipment.

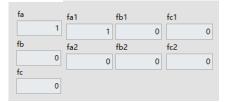


Figure 7: Inverter fault flag during S_{A1} short circuit fault.

Taking phase A as an example, simulate a high voltage fault in the power grid, as shown in Figure 8. Figure 9 shows the indication results of the fault flag. The fault flag fa2 of phase A is 1, and the other fault flags are 0. The results are correct.

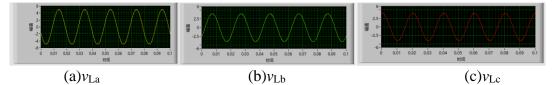


Figure 8: Measured voltage of power grid during A-phase voltage is too high.

fb1		fc1	
	0		0
fb2		fc2	
	0		0
		0 0 fb2	0 0 fb2 fc2

Figure 9: Power grid fault flag during A-phase voltage is too high.

Taking phase A as an example, simulate a low voltage fault in the power grid, as shown in Figure 10. Figure 11 shows the indication results of the fault flag. The fault flag fa1 of phase A is 1, and the other fault flags are 0. The results are correct.

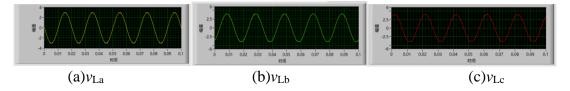


Figure 10: Measured voltage of power grid during A-phase voltage is too low.

fa1		fb1		fc1	
	1		0		0
fa2		fb2		fc2	
	0		0		0

Figure 11: Power grid fault flag during A-phase voltage is too low.

Taking phase A as an example, simulate a phase missing fault in the power grid, as shown in Figure 12. Figure 13 shows the indication results of the fault flag. The fault flag fa of phase A is 1, and the other fault flags are 0. The results are correct.

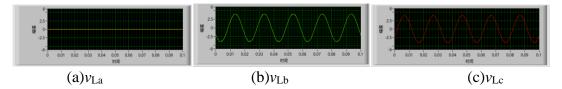


Figure 12: Measured voltage of power grid during A phase missing.

fa		fb		fc	
	1		0		0

Figure 13: Power grid fault flag during A phase missing.

Simulate midpoint potential imbalance, and Figure 12 shows that the fault flag fo is 1. The results are correct.



Figure 14: Midpoint potential imbalance flag during imbalance.

5 Conclusions

This article proposes a fault diagnosis algorithms for high speed maglev traction inverter system based on the analytical model, which effectively extracts and accurately locates the fault characteristics under all operating conditions. By combining fault diagnosis equipment, online parameter monitoring and rapid fault diagnosis have been achieved. This provides theoretical basis and practical experience support for the application of fault diagnosis technology in high speed maglev traction inverter system.

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